

WE CLAIM:

1. A gate stack in an integrated circuit comprising a PMOS region, an NMOS region, a dielectric layer, and a barrier layer, wherein the barrier layer overlies both the PMOS region and the NMOS region.
2. The gate stack of Claim 1, wherein the barrier layer is conductive.
3. The gate stack of Claim 1, wherein the barrier layer comprises a material selected from the group consisting of Ni, W, Pt, Co, TiN, TiAl_xN_y, TaN, TaAl_xN_y, Ru, RuO₂, Ir, IrO₂, HfN, HfAl_xN_y, WN_xC_y, and HfSi_xN_y.
4. The method of Claim 1, wherein the barrier layer is a nanolaminate.
5. The gate stack of Claim 1, wherein the barrier layer is less than about 100 angstroms thick.
6. The gate stack of Claim 5, wherein the barrier layer is less than about 50 angstroms thick.
7. The gate stack of Claim 1, additionally comprising a first gate electrode layer and a second gate electrode layer.
8. The gate stack of Claim 7, wherein the first gate electrode layer and the second gate electrode layer are adjacent.
9. The gate stack of Claim 7, wherein the first gate electrode layer comprises a first gate electrode material and the second gate electrode layer comprises a second gate electrode material.
10. The gate stack of Claim 9, wherein the first gate electrode material and the second gate electrode material are conductive.
11. The gate stack of Claim 9, wherein the first gate electrode material is different from the second gate electrode material.
12. The gate stack of Claim 7, wherein the first gate electrode layer overlies the PMOS region and the second gate electrode layer overlies the NMOS region.
13. The gate stack of Claim 12, wherein the work function of a transistor defined in the PMOS region of the gate stack is determined by the first gate electrode material.
14. The gate stack of Claim 12, wherein the work function of a transistor defined in the NMOS region of the gate stack is determined by the second gate electrode material.

15. A method of forming a gate stack in an integrated circuit comprising:
depositing a dielectric layer over a substrate comprising a first region and a second region;
depositing a barrier layer directly over the dielectric layer such that it overlies both the first and second regions; and
forming a first gate electrode layer over the first region of the substrate and a second gate electrode layer over the second region.
16. The method of Claim 15, wherein the first region is a PMOS region and the second region is an NMOS region.
17. The method of Claim 15, wherein the first and second gate electrode layers are adjacent to each other
18. The method of Claim 15, wherein the first gate electrode layer comprises a first gate electrode material and the second gate electrode layer comprises a second gate electrode material.
19. The method of Claim 18, wherein the first and second gate electrode materials are conductive.
20. The method of Claim 18, wherein the first and second gate electrode materials are different.
21. The method of Claim 18, wherein the first and second gate electrode materials are selected from the group consisting of poly-silicon, Ti, Ni, Al, W, Pt, Co, TiN, TiAl_xN_y , TaN, TaAl_xN_y , Ru, RuO_2 , Ir, IrO_2 , HfN, WN_xC_y , HfAl_xN_y and HfSi_xN_y .
22. The method of Claim 19 wherein either the first or second gate electrode material is a metal nitride.
23. The method of Claim 15, wherein the barrier layer comprises a conductive material.
24. The method of Claim 23, wherein the conductive material is selected from the group consisting of Ti, Ni, Al, W, Pt, Co, TiN, TiAl_xN_y , TaN, TaAl_xN_y , Ru, RuO_2 , Ir, IrO_2 , HfN, WN_xC_y , HfAl_xN_y and HfSi_xN_y .

25. The method of Claim 15, wherein the barrier layer is deposited by a process selected from the group consisting of ALD, CVD, MOCVD, plasma-enhanced ALD and plasma-enhanced CVD.

26. The method of Claim 25, wherein the barrier layer is deposited by ALD.

27. The method of Claim 15, wherein the barrier layer is deposited to a thickness of less than about 100 Å.

28. The method of Claim 27, wherein the barrier layer is deposited to a thickness of less than about 30 Å.

29. The method of Claim 15, additionally comprising treating the dielectric layer to remove OH groups on the surface prior to deposition of the barrier layer.

30. The method of Claim 29, wherein the dielectric layer is treated with ammonia gas.

31. The method of Claim 29, wherein the dielectric layer is treated with radicals.

32. The method of Claim 31, wherein the dielectric layer is treated with nitrogen-hydrogen plasma.

33. The method of Claim 15, wherein forming a first gate electrode layer over the first region comprises depositing a layer of first gate electrode material over the first and second regions of the substrate.

34. The method of Claim 33, wherein forming a first gate electrode layer over the first region additionally comprises removing first gate electrode material from over the second region of the substrate without removing the underlying barrier layer.

35. The method of Claim 34, wherein the first gate electrode material is removed from over the second region of the substrate by chemical mechanical polishing.

36. The method of Claim 34, wherein forming the second gate electrode layer comprises depositing a layer of second gate electrode material over the first and second regions of the substrate.

37. The method of Claim 34, wherein the first gate electrode material is removed from over the second region of the substrate by differential etching.

38. The method of Claim 37, wherein forming the second gate electrode layer over the second region comprises depositing a layer of second gate electrode material over

the first and second regions of the substrate and removing second gate electrode material from over the first region without removing the underlying barrier layer.

39. The method of Claim 15, additionally comprising depositing a layer of conductive material over the first and second gate electrode layers.

40. The method of Claim 15, wherein forming a first gate electrode over the first region of the substrate comprises etching the barrier layer over the second region to a thickness of no more than about 100 angstroms.

41. The method of Claim 40, wherein forming a second gate electrode over the second region of the substrate comprising depositing a layer of conductive material over the second region.

42. A method of forming a first and second electrode in an integrated circuit comprising:

- depositing a dielectric layer over a substrate comprising a first region and a second region;

- depositing a barrier layer directly over the dielectric layer such that it overlies the first and second regions;

- depositing a first gate electrode material over the first and second regions of the substrate;

- removing first gate electrode material from over the first region without removing the barrier layer; and

- depositing a second gate electrode material over the substrate, and
defining a first and second electrode in the first and second region.